CLAIMS

What is claimed is:

1. A processor surrogate for use in a processing node of a multiprocessor data processing system having a plurality of processing nodes coupled together and to a plurality of input/output devices using corresponding communication links, the processor surrogate comprising:

    a first port comprising a first set of integrated circuit terminals adapted to be coupled to a first external communication link for coupling to one of the plurality of processing nodes;

    a second port comprising a second set of integrated circuit terminals adapted to be coupled to a second external communication link for coupling to one of the plurality of input/output devices; and

    an interconnection circuit coupled between said first port and said second port.

2. The processor surrogate of claim 1 wherein said interconnection circuit comprises a passive interconnection between said first port and said second port.

3. The processor surrogate of claim 2 wherein said interconnection circuit further comprises:

    a first set of internal connections between a plurality of input terminals of said first port and a corresponding plurality of output terminals of said second port; and

    a second set of internal connections between a plurality of input terminals of said second port and a corresponding plurality of output terminals of said first port.

4. The processor surrogate of claim 1 wherein said interconnection circuit comprises an active interconnection between said first port and said second port.

5. The processor surrogate of claim 4 wherein said interconnection circuit further comprises:

a first communication link controller coupled to said first port;

a second communication link controller coupled to said second port; and

a crossbar switch having a first terminal coupled to said first communication link controller, and a second terminal coupled to said second communication link controller.

6. The processor surrogate of claim 5 wherein said interconnection circuit further comprises:

a memory controller coupled to said crossbar switch and adapted to be coupled to an external memory, for controlling accesses between said first and second communication link controllers and said external memory.

7. The processor surrogate of claim 5 wherein said first and second communication link controllers are substantially compatible with the HyperTransport™ I/O Link Specification, Revision 1.05.

8. The processor surrogate of claim 7 wherein said first communication link controller implements a coherent form of the HyperTransport™ I/O Link Specification, Revision 1.05.

9. A processor surrogate for use in a multiprocessor data processing system having a first processing node including an actual processor and a second processing node coupled to the first processing node and including the processor surrogate, the processor surrogate comprising:

an integrated circuit package having a first plurality of terminals forming a first port of the processor surrogate and disposed at locations corresponding to a first link controller of the actual processor, and a second plurality of terminals forming a second port of the processor surrogate and disposed at locations corresponding to a second link controller of the actual processor; and

a plurality of electrical connections between said first plurality of terminals of said first port and corresponding ones of said second plurality of terminals of said second port.

10. The processor surrogate of claim 9 wherein said plurality of electrical connections comprises:

a first set of internal connections between a plurality of input terminals of said first port and a corresponding plurality of output terminals of said second port; and

a second set of internal connections between a plurality of input terminals of said second port and a corresponding plurality of output terminals of said first port.

11. The processor surrogate of claim 9 wherein said first and second link controllers of the actual processor are substantially compatible with the HyperTransport™ I/O Link Specification, Revision 1.05.

12. The processor surrogate of claim 9 wherein the multiprocessor data processing system further comprises an input/output device coupled to said second port of the processor surrogate .

13. A processor surrogate for use in a multiprocessor data processing system having a plurality of processing nodes comprising a first processing node including an actual processor and a second processing node coupled to the first processing node and including the processor surrogate, the processor surrogate comprising:

a first port comprising a first set of integrated circuit terminals adapted to be coupled to a first external communication link and thereby to one of the plurality of processing nodes;

a second port comprising a second set of integrated circuit terminals adapted to be coupled to a second external communication link and thereby to an input/output device; and

an active interconnection circuit coupled between said first port and said second port to thereby couple said one of the plurality of processing nodes and said input/output device.

14. The processor surrogate of claim 13 wherein said one of the plurality of processing nodes comprises said first node including said actual processor.

15. The processor surrogate of claim 13 wherein said active interconnection circuit comprises:

a first communication link controller coupled to said first port;

a second communication link controller coupled to said second port; and

a crossbar switch having a first terminal coupled to said first communication link controller, and a second terminal coupled to said second communication link controller.

16. The processor surrogate of claim 15 further comprising:

a memory controller coupled to said crossbar switch and adapted to be coupled to an external memory, for controlling accesses between said first and second communication link controllers and said external memory.

17. The processor surrogate of claim 15 wherein said first and second communication link controllers are substantially compatible with the HyperTransport™ I/O Link Specification, Revision 1.05.

18. The processor surrogate of claim 17 wherein said first communication link controller implements a coherent form of the HyperTransport™ I/O Link Specification, Revision 1.05.

19. The processor surrogate of claim 13 further comprising:

a third port comprising a third set of integrated circuit terminals coupled to said active interconnection circuit and adapted to be coupled to a third external communication link and thereby to a second input/output device.

20. A multiprocessor data processing system comprising:

a first processing node comprising an actual processor;

a second processing node comprising a processor surrogate having a first port coupled to said first processing node, a second port, and an interconnection circuit coupled between said first port and said second port; and

an input/output device coupled to said second port of said second processing node and accessible to said actual processor via said processor surrogate.

21. The multiprocessor data processing system of claim 20 wherein said interconnection circuit comprises a passive interconnection between said first port and said second port.

22. The multiprocessor data processing system of claim 21 wherein said interconnection circuit further comprises:

a first set of internal connections between a plurality of input terminals of said first port and a corresponding plurality of output terminals of said second port; and

a second set of internal connections between a plurality of input terminals of said second port and a corresponding plurality of output terminals of said first port.

23. The multiprocessor data processing system of claim 20 wherein said interconnection circuit comprises an active interconnection between said first port and said second port.

24. The multiprocessor data processing system of claim 23 wherein said interconnection circuit further comprises:

a first communication link controller coupled to said first port;

a second communication link controller coupled to said second port; and

a crossbar switch having a first terminal coupled to said first communication link controller, and a second terminal coupled to said second communication link controller.

25. The multiprocessor data processing system of claim 24 wherein said first and second communication link controllers are substantially compatible with the HyperTransport™ I/O Link Specification, Revision 1.05.

26. The multiprocessor data processing system of claim 24 wherein said first communication link controller implements a coherent form of the HyperTransport™ I/O Link Specification, Revision 1.05.

27. The multiprocessor data processing system of claim 24 further comprising:

a memory controller coupled to said crossbar switch and adapted to be coupled to an external memory, for controlling accesses between said first and second communication link controllers and said external memory.

28. A multiprocessor data processing system comprising:

a first processing node comprising an actual processor;

a second processing node comprising a first processor surrogate having a first port coupled to said first processing node, a second port, a third port, and an interconnection circuit coupled between said first port, said second port, and said third port;

a third processing node coupled to said third port of said first processor surrogate in said second processing node;

a fourth processing node coupled to said third processing node and to said first processing node; and

a first input/output device coupled to said second port of said second processing node and accessible to said actual processor via said first processor surrogate.

29. The multiprocessor data processing system of claim 28 wherein said third processing node comprises a second processor surrogate having a first port coupled to said third port of said first processor surrogate in said second processing node, a second port, a third port coupled to said fourth processing node, and an interconnection circuit coupled between said first port, said second port, and said third port thereof.

30. The multiprocessor data processing system of claim 29 further comprising:

a second input/output device coupled to said second port of said second processor surrogate and accessible to said actual processor via said first processor surrogate and said second processor surrogate.

31. The multiprocessor data processing system of claim 30 wherein said fourth processing node comprises a third processor surrogate having a first port coupled to said third processing node, a second port, a third port coupled to said first processing node, and an interconnection circuit coupled between said first port, said second port, and said third port thereof.

32. The multiprocessor data processing system of claim 31 further comprising:

a third input/output device coupled to said second port of said third processor surrogate and accessible to said actual processor via said third processor surrogate.